

1 We claim:

2

3

4 1) A signal processing system for a wireless  
5 communications system, said signal processing system  
6 comprising:

7 a baseband receiver having one or more control inputs  
8 and a status output;

9 a transmit modulator having a quadrature input, one or  
10 more control inputs, and a status output;

11 a baseband receive processor having one or more control  
12 outputs;

13 a baseband transmit processor having a quadrature  
14 output, a control output, and a transmit enable output;

15 a first multiplexer having an output, said output  
16 selecting either:

17 one of said baseband receive processor control outputs

18 or one of said baseband transmit processor quadrature  
19 outputs , said first multiplexer making a selection based on  
20 said transmit enable, said first multiplexer output coupled  
21 to a first digital to analog converter (DAC), said first DAC  
22 output coupled to one of said transmit modulator quadrature  
23 inputs and also to one of said baseband receiver control  
24 inputs;

1        a second multiplexer having an output, said output  
2        selecting either:  
3        other said baseband receive processor control output or  
4        the other of said baseband transmit processor quadrature  
5        output, said second multiplexer making a selection based on  
6        said transmit enable, said second multiplexer output coupled  
7        to a second digital to analog converter (DAC), and  
8        delivering said second DAC output to the other of said  
9        transmit modulator quadrature inputs and also to the other  
10       of said baseband receiver control inputs;  
11       a third multiplexer having an output, said output  
12       selecting either said baseband receiver status signal or  
13       said transmit modulator status signal, said third  
14       multiplexer output making a selection based on said transmit  
15       enable, said third multiplexer output coupled to a first  
16       analog to digital converter, the output of said analog to  
17       digital converter coupled to said baseband receive processor  
18       status signal and also to said baseband transmit processor  
19       status signal.

20

21       2) The signal processing system of claim 1 where said  
22       first multiplexer couples one of said baseband receive  
23       processor control signals to said first DAC when said  
24       transmit enable is not active.

25

1           3) The signal processing system of claim 2 where said  
2 baseband receive processor control signal is a gain control  
3 signal.

4

5           4) The signal processing system of claim 1 where said  
6 first multiplexer couples one of said baseband transmit  
7 processor quadrature signals to said first DAC when said  
8 transmit enable is active.

9

10          5) The signal processing system of claim 1 where said  
11 second multiplexer couples one of said baseband receive  
12 processor control signals to said second DAC when said  
13 transmit enable is not active.

14

15          6) The signal processing system of claim 5 where said  
16 baseband receive processor control signal is a gain control  
17 signal.

18

19          7) The signal processing system of claim 1 where said  
20 second multiplexer couples one of said baseband transmit  
21 processor quadrature signals to said second DAC when said  
22 transmit enable is active.

23

1           8) The signal processing system of claim 1 where said  
2 third multiplexer couples said baseband receiver status  
3 signal to said ADC when said transmit enable is not active.

4  
5           9) The signal processing system of claim 8 where said  
6 baseband receiver status signal is receive signal strength  
7 indication.

8  
9           10) The signal processing system of claim 1 where said  
10 third multiplexer couples said transmit modulator status  
11 signal to said third ADC when said transmit signal is  
12 active.

13  
14           11) The signal processing system of claim 10 where said  
15 transmit modulator status signal is a transmit power  
16 strength.

17  
18           12) The signal processing system of claim 1 where at  
19 least one of said baseband receive processor or said  
20 baseband transmit processor is a digital circuit.

21  
22           13) The signal processing system of claim 12 where said  
23 digital circuit is an integrated circuit.

24

1        14) The signal processing system of claim 12 where said  
2 digital circuit is a field programmable gate array (FPGA).

3

4        15) A signal processing system for a wireless  
5 communications system, said signal processing system  
6 comprising:

7        a baseband receiver having one or more control inputs  
8 and a status output;

9        a transmit modulator having a quadrature input, one or  
10 more control inputs, and a status output;

11       a baseband receive processor having one or more control  
12 outputs;

13       a baseband transmit processor having a quadrature  
14 output, a control output, and a transmit enable output;

15       a first multiplexer having an output, said output  
16 selecting one of:

17       said baseband receive processor control output or one  
18 of said baseband transmit processor quadrature outputs, said  
19 first multiplexer making a selection based on said transmit  
20 enable, said first multiplexer output coupled to a first  
21 digital to analog converter (DAC), said first DAC output  
22 coupled to one of said transmit modulator quadrature inputs  
23 and also to one of said baseband receiver control inputs;

24       a second multiplexer having an output, said output  
25 selecting either:

1        other said baseband receive processor control output or  
2 the other of said baseband transmit processor quadrature  
3 outputs, said second multiplexer making a selection based on  
4 said transmit enable, said second multiplexer output coupled  
5 to a second digital to analog converter (DAC), and  
6 delivering said second DAC output to the other of said  
7 transmit modulator quadrature inputs and also to the other  
8 of said baseband receiver control inputs.

9

10        16) The signal processing system of claim 15 where said  
11 first multiplexer couples one of said baseband receive  
12 processor control signals to said first DAC when said  
13 transmit enable is not active.

14

15        17) The signal processing system of claim 16 where said  
16 baseband receive processor control signal is a gain control  
17 signal.

18

19        18) The signal processing system of claim 15 where said  
20 first multiplexer couples one of said baseband transmit  
21 processor quadrature signals to said first DAC when said  
22 transmit enable is active.

23

24        19) The signal processing system of claim 15 where said  
25 second multiplexer couples one of said baseband receive

1 processor control signals to said second DAC when said  
2 transmit enable is not active.

3

4 20) The signal processing system of claim 19 where said  
5 baseband receive processor control signal is a gain control  
6 signal.

7

8 21) The signal processing system of claim 15 where said  
9 second multiplexer couples one of said baseband transmit  
10 processor quadrature signals to said second DAC when said  
11 transmit enable is active.

12

13 22) The signal processing system of claim 1 or 15 where  
14 said baseband receiver quadrature outputs and said transmit  
15 modulator quadrature input signals are analog signals.

16

17 23) The signal processing system of claim 1 or 15 where  
18 said baseband receive processor quadrature inputs and said  
19 baseband transmit processor outputs are digital signals  
20 having more than one bit of width.

21

22 24) A signal processing system for a wireless  
23 communications system, said signal processing system  
24 comprising:

1       a baseband receiver having one or more control inputs,  
2       quadrature outputs, and a status output;  
3       a transmit modulator having a quadrature input, one or  
4       more control inputs, and a status output;  
5       a baseband receive processor having one or more control  
6       outputs, a multiplexer control, and a quadrature input;  
7       a baseband transmit processor having a quadrature  
8       output, a sample output, and a transmit enable output;  
9       a first multiplexer having an output which selects  
10      between one of:  
11        said baseband receive processor control outputs or one  
12      of said baseband transmit processor quadrature outputs in  
13      response to said transmit enable, said first multiplexer  
14      output coupled to a first digital to analog converter (DAC),  
15      and delivering said first DAC output to one of said transmit  
16      modulator quadrature inputs and also to one of said baseband  
17      receiver control inputs;  
18       a sample and hold having an input coupled to said first  
19      DAC output and an output coupled to one of said transmit  
20      modulator control signals, said sample and hold controlled  
21      by said baseband transmit processor said sample output;  
22       a second multiplexer having an output, said second  
23      multiplexer output coupled to one of:  
24        other said baseband receive processor control output or  
25      the other of said baseband transmit processor quadrature



1 output in response to said transmit select, said second  
2 multiplexer output coupled to a second digital to analog  
3 converter (DAC) and delivering said second DAC output to the  
4 other of said transmit modulator quadrature inputs and also  
5 to the other of said baseband receiver control inputs;  
6 a third multiplexer having an output, said third  
7 multiplexer output coupled to either of:  
8 one of said baseband receiver quadrature outputs or  
9 said baseband receiver status signal in response to said  
10 baseband receiver processor said multiplexer control, said  
11 third multiplexer output coupled to a first analog to  
12 digital converter, the output of said analog to digital  
13 converter coupled to said baseband receive processor status  
14 signal and also to one of said baseband receiver quadrature  
15 inputs;  
16 a fourth multiplexer having an output, said fourth  
17 multiplexer output coupled to one of:  
18 the other said baseband receiver quadrature output or  
19 said transmit modulator status signal, said fourth  
20 multiplexer selection controlled by said baseband transmit  
21 processor said transmit enable, said fourth multiplexer  
22 output coupled to a second analog to digital converter  
23 (ADC), the output of said second ADC coupled to the other  
24 said receive processor quadrature input and said baseband  
25 transmit processor status signal.

1

2        25) The signal processing system of claim 24 where said  
3 first multiplexer couples one of said baseband receive  
4 processor control signals to said first DAC when said  
5 transmit enable is not active.

6

7        26) The signal processing system of claim 25 where said  
8 baseband receive processor control signal is a gain control  
9 signal.

10

11       27) The signal processing system of claim 24 where said  
12 first multiplexer couples one of said baseband transmit  
13 processor quadrature signals to said first DAC when said  
14 transmit enable is active.

15

16       28) The signal processing system of claim 24 where said  
17 second multiplexer couples one of said baseband receive  
18 processor control signals to said second DAC when said  
19 transmit enable is not active.

20

21       29) The signal processing system of claim 28 where said  
22 baseband receive processor control signal is a gain control  
23 signal.

24

1           30) The signal processing system of claim 24 where said  
2 second multiplexer couples one of said baseband transmit  
3 processor quadrature signals to said second DAC when said  
4 transmit enable is active.

5  
6           31) The signal processing system of claim 24 where said  
7 third multiplexer couples said baseband receiver status  
8 signal to said ADC when said receive processor said  
9 multiplexer control is not active.

10  
11           32) The signal processing system of claim 31 where said  
12 baseband receiver status signal is receive signal strength  
13 indication.

14  
15           33) The signal processing system of claim 24 where said  
16 third multiplexer couples one of said baseband receiver  
17 quadrature outputs to said first ADC when said receiver  
18 processor said multiplexer control is active.

19  
20           34) The signal processing system of claim 24 where a  
21 transmit gain value is placed on one of said baseband  
22 transmit processor quadrature outputs and said sample output  
23 is active.

1        35) The signal processing system of claim 24 where at  
2        least one of said baseband receive processor or said  
3        baseband transmit processor is a digital circuit.

4  
5        36) The signal processing system of claim 35 where said  
6        digital circuit is an integrated circuit.

7  
8        37) The signal processing system of claim 35 where said  
9        digital circuit is a field programmable gate array (FPGA).

10  
11       38) The signal processing system of claim 1 where said  
12       first multiplexer includes a test input which is coupled to  
13       said first DAC or to said DAC, selectable by said transmit  
14       enable.

15  
16       39) The signal processing system of claim 1 where said  
17       second multiplexer includes a test input which is coupled to  
18       said first DAC or to said second DAC, selectable by said  
19       transmit enable.

20  
21       40) The signal processing system of claim 15 where said  
22       first multiplexer includes a test input which is coupled to  
23       said first DAC or to said DAC, selectable by said transmit  
24       enable.

25

1           41) The signal processing system of claim 15 where said  
2 first multiplexer includes a test input which is coupled to  
3 said first DAC or to said DAC, selectable by said transmit  
4 enable.

5

6

7           42) The signal processing system of claim 24 where said  
8 third multiplexer includes a test input which is coupled to  
9 said first DAC or to said DAC.

10

11

12           43) The signal processing system of claim 24 where said  
13 fourth multiplexer includes a test input which is coupled to  
14 said first DAC or to said DAC.

15

16

17